



# **Effects of Specialized Clock Routing on Clock Tree Timing, Signal Integrity, and Routing Congestion**

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# Overview

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- Why avoid capacitive coupling on the clock tree?
- What methods exist for avoiding coupling?
- How well do those methods work?
- What are the impacts of using each method when hardening IP?



# Clock Tree Routing Goals

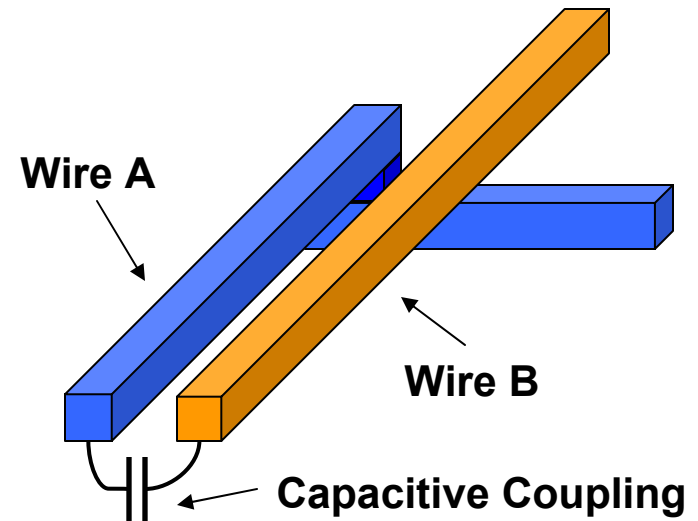
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1. Ensure a high quality clock tree post routing with minimal skew and latency
2. Decrease the overall amount of coupling capacitance between the clock nets and any other net in the design (including powers)
3. Use the least amount of routing resources to wire the clock nets

# Capacitive Coupling

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- Capacitive coupling causes delay, and signal integrity issues
- Coupling capacitance can only truly be measured after detailed routing
  - It is difficult to predict
- Effects of coupling are most difficult to fix after detailed routing
- Clock nets are strong coupling noise aggressors – would like to prevent coupling
- Crosstalk on clock nets reduces pulse-widths, induces glitches, increases skew, adds jitter





# The 5 Techniques

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- Traditional Clock Routing
- Clock Routing Isolation
- Shielded Clock Routes
- Isolation with the Power Grid
- Active Mitigation



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# Experimental Method

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- All 5 techniques are run on that same design, same placement, same clock tree
- Skew and latency are measured after a full routing
- Astro used for skew and latency measurements
- Star-RCXT used to measure capacitive coupling
- For techniques involving isolation or shielding a weakened version of the experiment was run
- The weakened version starts from the non-weakened version, removes the isolation/shielding constraint, and runs incremental routing

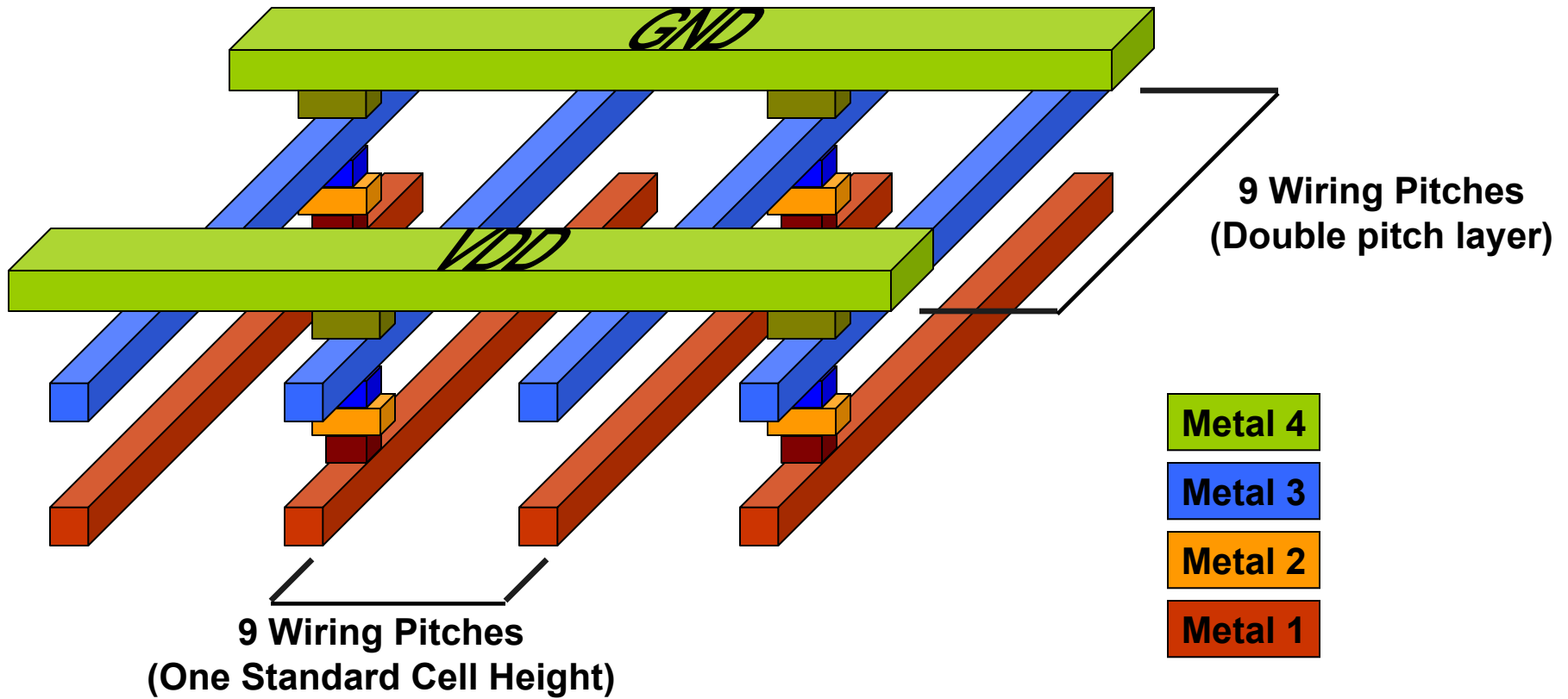
# Design Used for Experimentation

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- Popular embedded processor
- Desire smallest design possible
- 0.13 $\mu$ m fabrication technology
- Less than .5 mm<sup>2</sup> in total area
- 179 clock gates controlling 2,328 D-type flip-flops
- 4<sup>th</sup> metal layer is double thick/double pitch
- Highly utilized circuit rows, only four routing layers, robust fine-grained power grid, and 4<sup>th</sup> metal layer being thick make routing the greatest design challenge

# Power Grid





# Traditional Routing

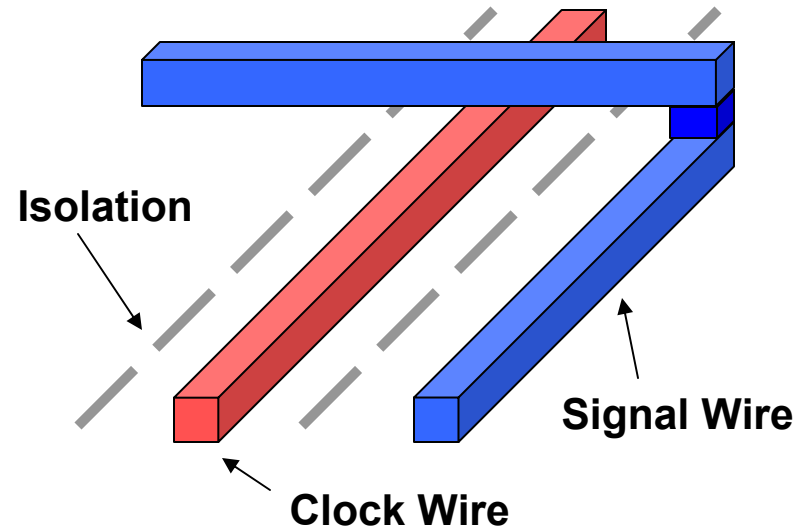
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- No specialized method used for routing clock nets except to balance routes for skew
- Standard method for earlier technologies
- Clock routes constrained to use only metals 3 & 4
- Metals 1 & 2 used for pin access
- Clocks routed prior to routing signal nets (enables better balancing)

# Isolated Routing

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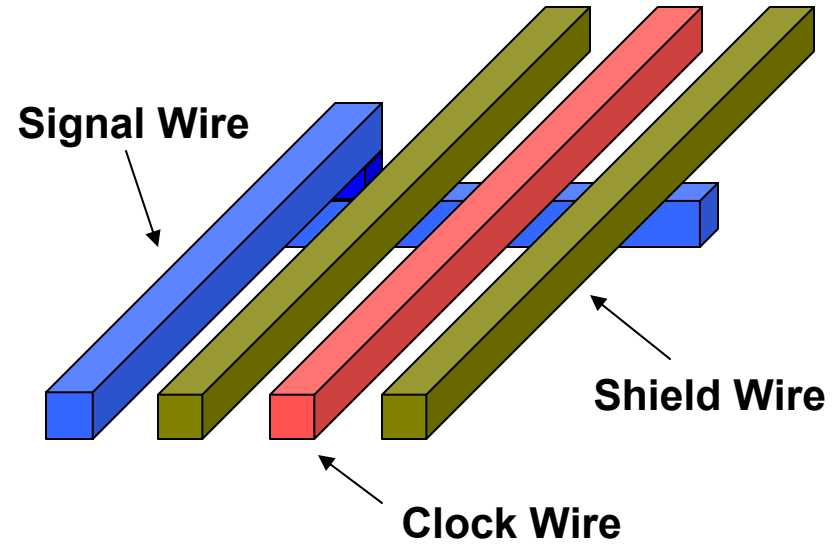
- 1 track of isolation on metals 3 & 4
- Clock constrained to metals 3 & 4
- Clock uses metals 1 & 2 for pin access
- Coupling capacitance still occurs between wires greater than one track away
- Difficult to predict coupling capacitance prior to detailed wiring



# Shielded Routing

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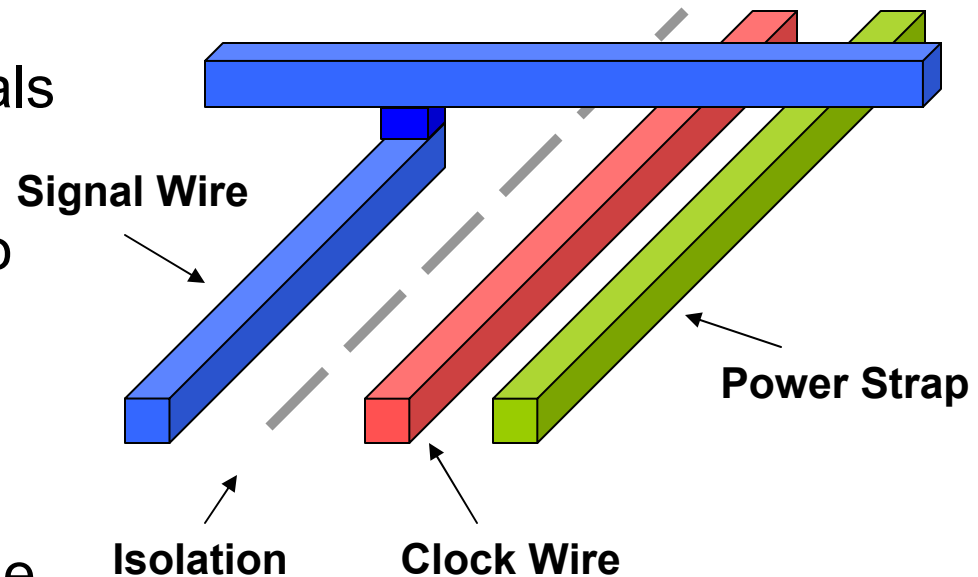
- 1 minimum width wire used to shield on each side of the clock wires only on metals 3 & 4
- Clock constrained to metals 3 & 4
- Metals 1 & 2 used for pin access with no shielding
- No coupling capacitance between wires outside of the shields
- Coupling capacitance between shield and clock wire
- Very predictable amount of coupling



# Isolation with the Power Grid

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- 1 track of isolation on metals 3 & 4
- Power straps allowed inside isolation
- Clock wires constrained to metals 3 & 4
- Clock wires only allowed next to power straps on metals 3 & 4
- Combination of isolation and shielding
- Uses the power grid to shield the clock wires
- Moderately predictable amount of coupling capacitance



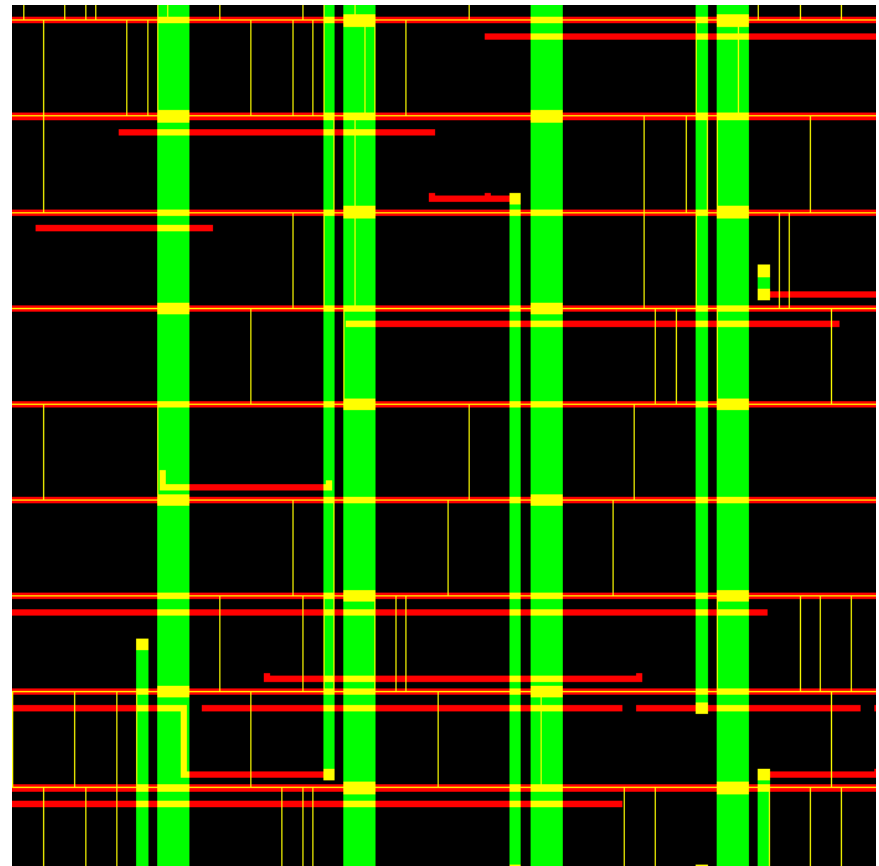
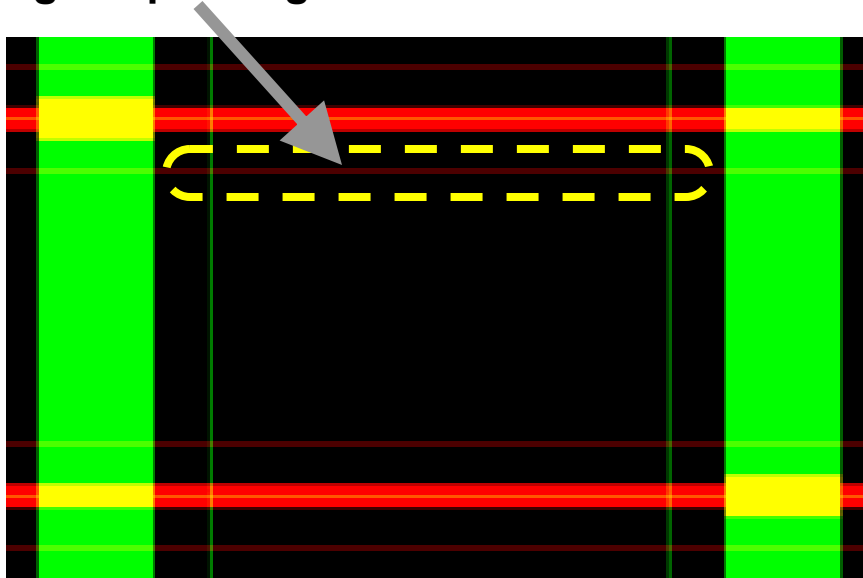


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# Implementation in Astro

1. Delete all wire tracks not adjacent to power on upper metal layers
2. Constrain clock routes to those layers
3. Route the clock nets
4. Add back in all the wiring tracks

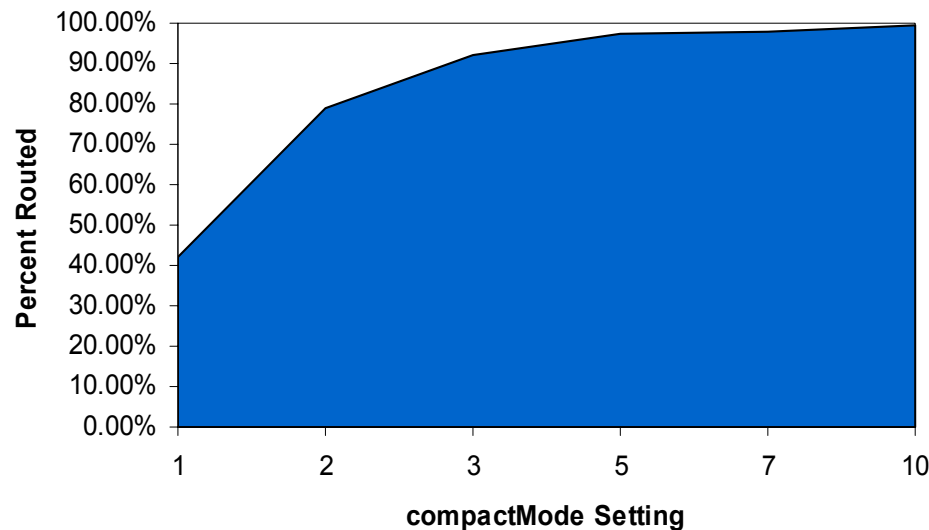
**Routing tracks only along the power grid**



# Effects of a Coarse Grained Power Grid

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- Experiment using previous method with only 25% of the original power grid
- Less power straps means fewer tracks for routing the clocks, greater distance between those tracks
- Astro global router & track assignment use a window when searching for tracks
- The compactMode parameters controls this windows size
- No valid setting allowed for 100% of clock nets to route with 0 DRCs
- Latency and skew increased dramatically
- **Isolation with the power grid only works if you have a fine-grained power grid**

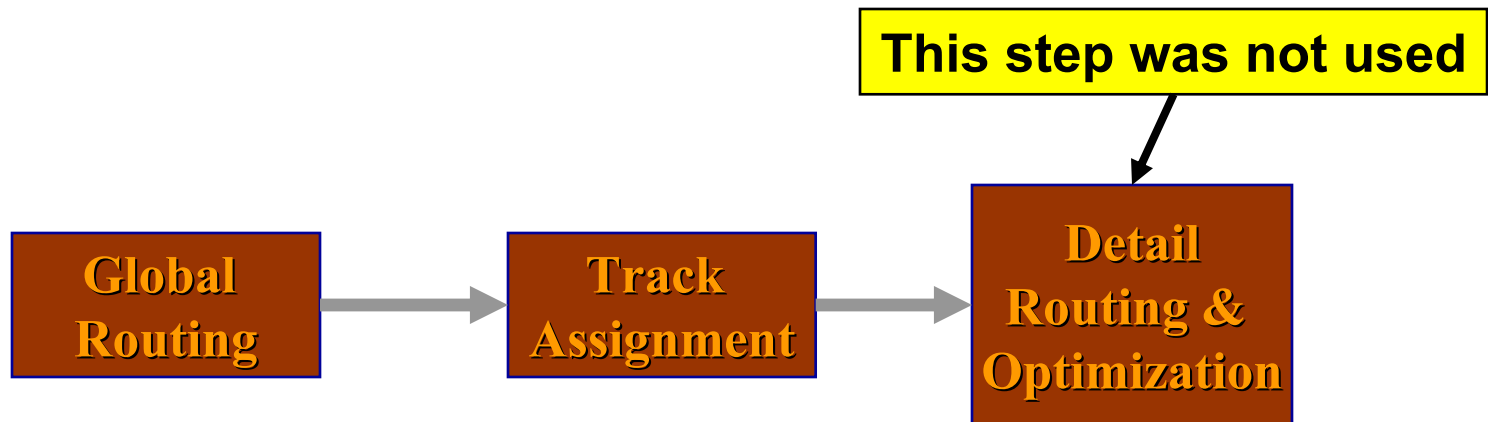


# Active Mitigation –Astro Xtalk

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- Identify Xtalk-sensitive nets
- Keep apart wires with overlapping timing windows
- Avoid assigning long parallel wires on adjacent tracks
- Reduce aggressor standard cell drive strength

## Astro Xtalk Flow



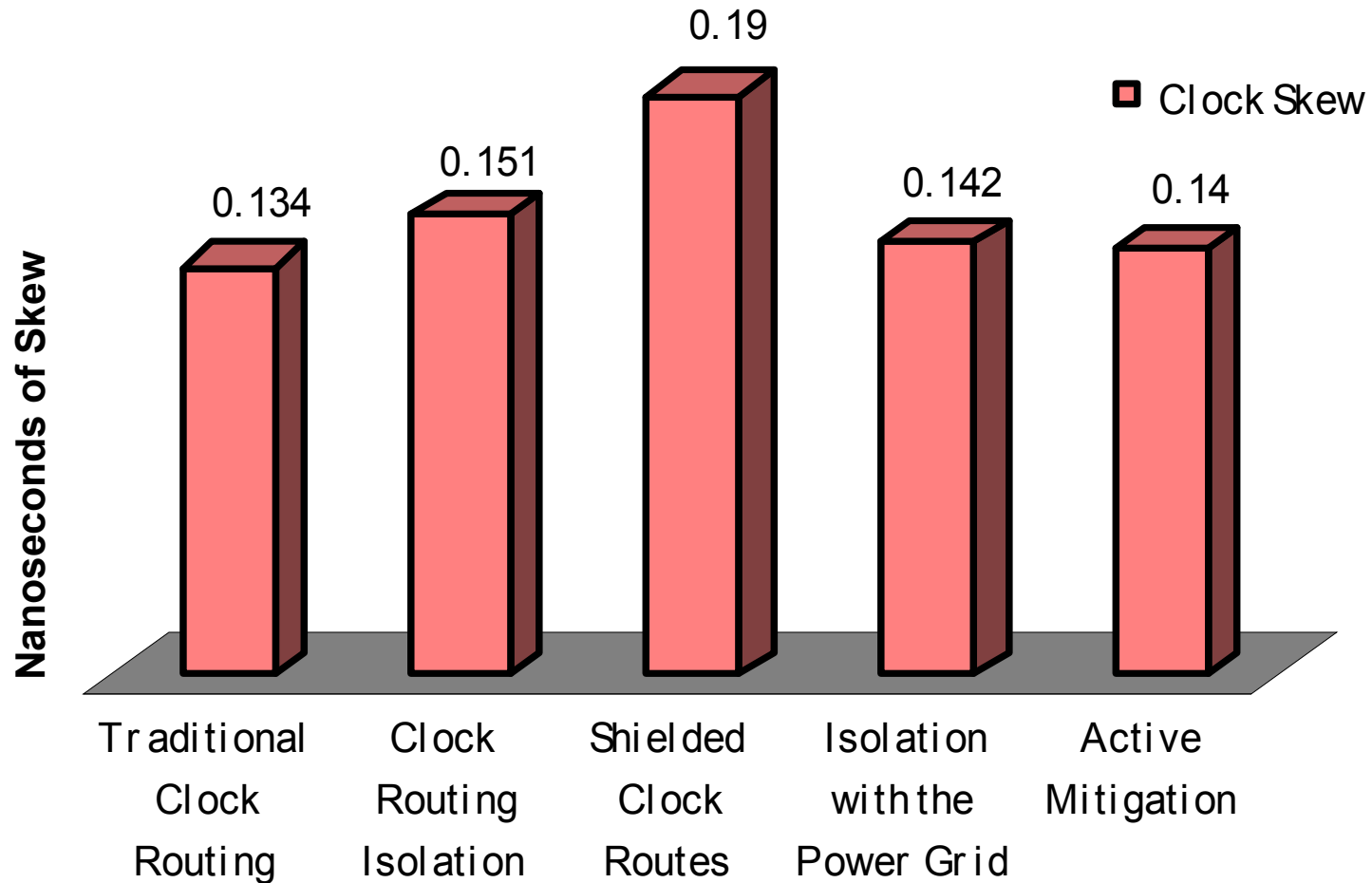


# Results – Overview

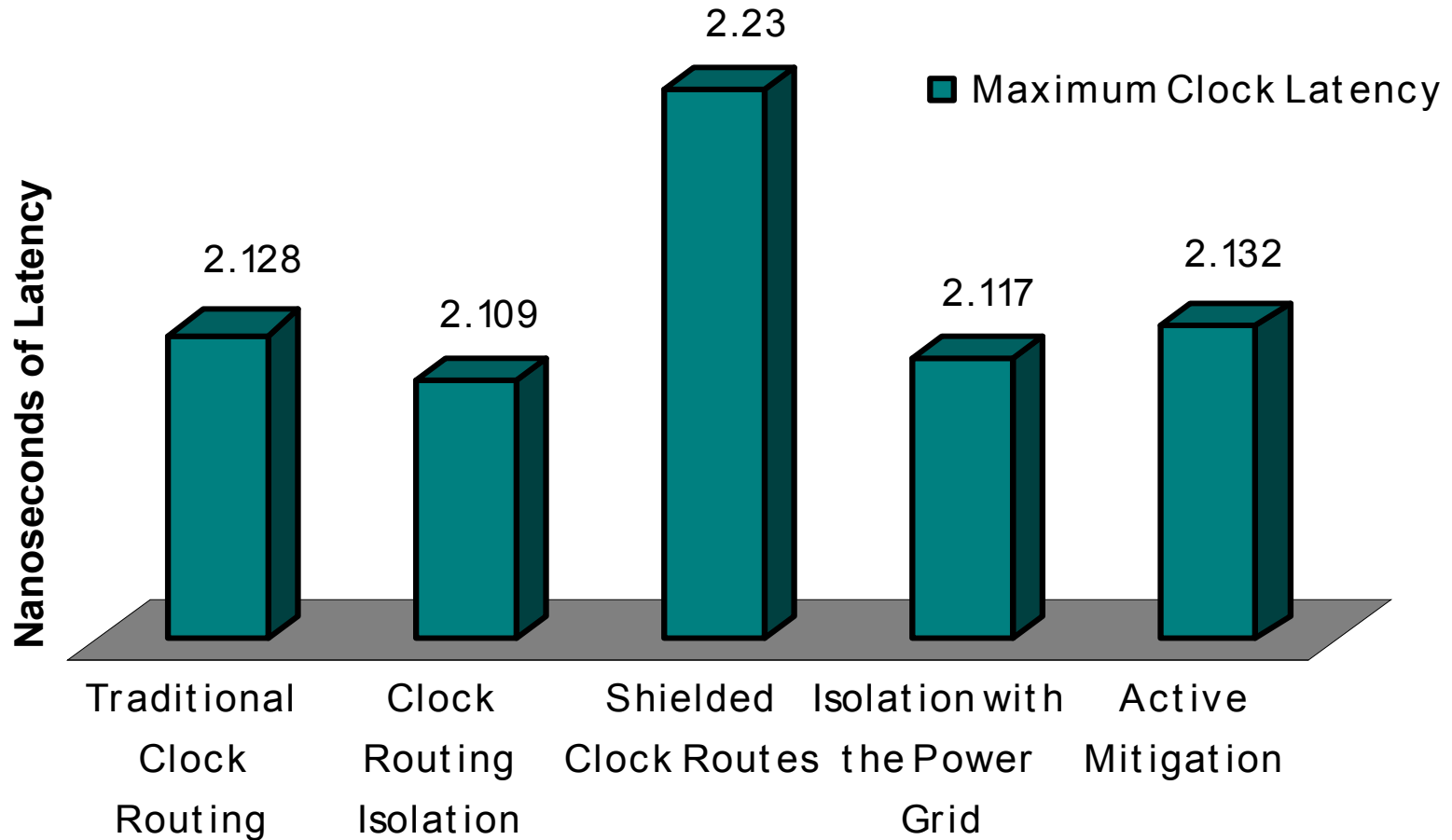
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- Clock Tree Quality: Skew and Latency
- Routability: Post-Routing DRC Violations
- Signal Coupling Avoidance: Aggregate Signal ↔ Clock Wire Coupling

# Clock Tree Quality – Skew



# Clock Tree Quality – Latency

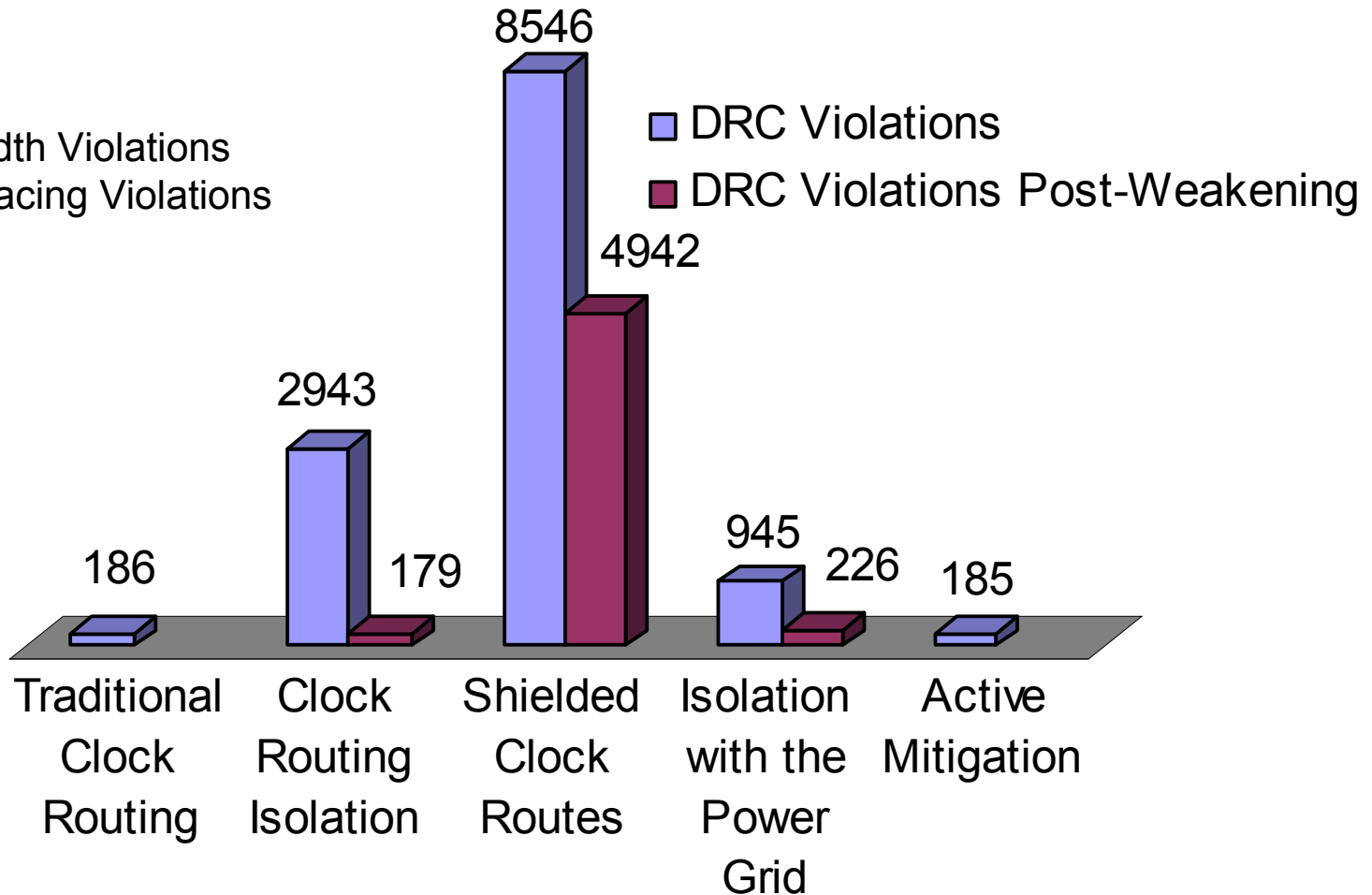




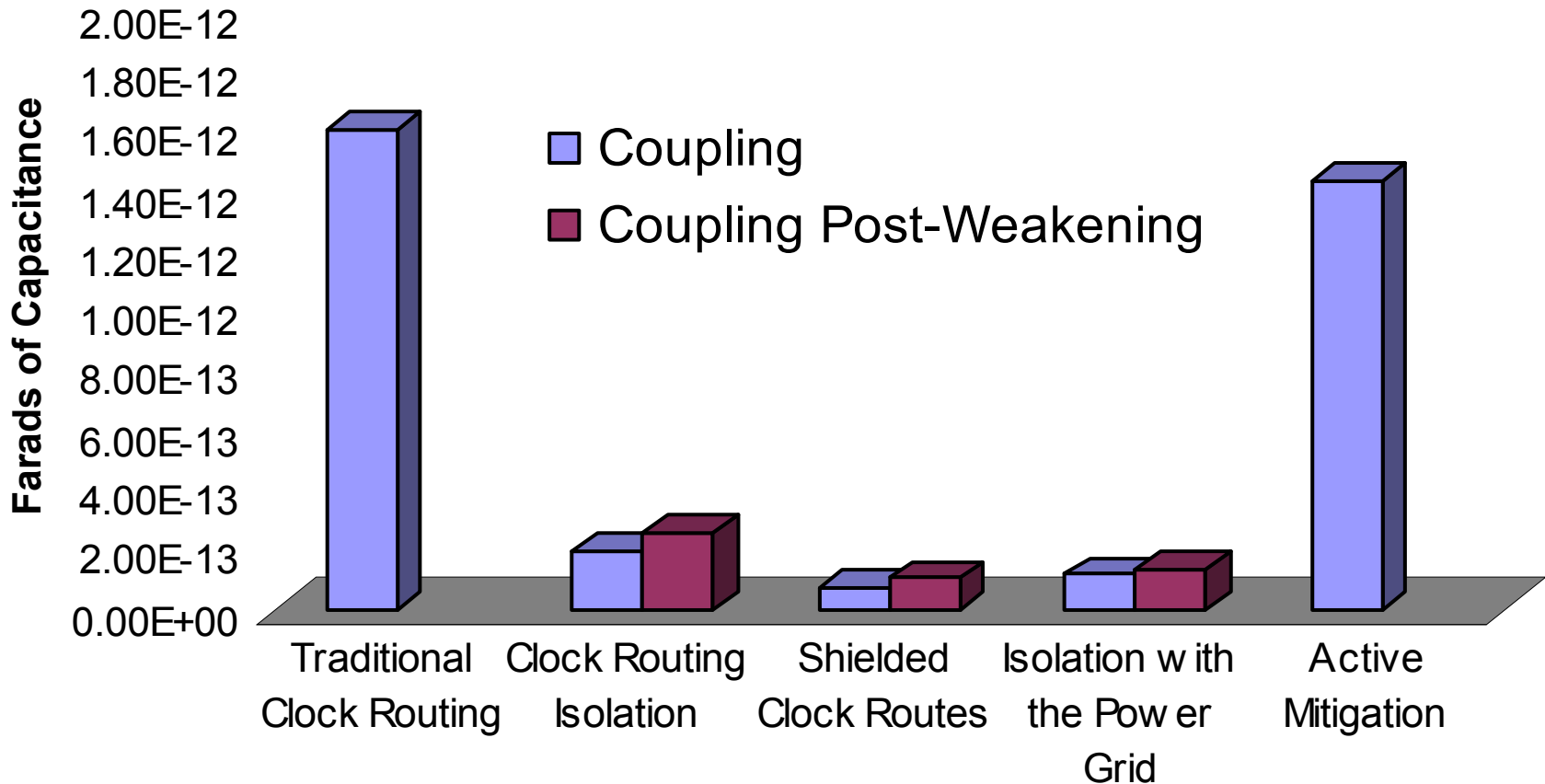
# Routability – DRC Violations

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- Shorts
- Opens
- Minimum Width Violations
- Minimum Spacing Violations
- Notch
- Etc....



# Coupling Avoidance – Aggregate Signal to Clock Coupling





# Summary of the Methods

Method	Clock Tree Quality	Design Routability	Capacitive Coupling Avoidance
Traditional Routes	Good	Excellent	Poor
Isolated Routes	Good	Moderate	Good
Shielded Routes	Moderate	Poor	Excellent
Isolation with the Power Grid	Good	Good	Good
Active Mitigation	Good	Excellent	Moderate