Jesse Craig

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RESEARCH INTERESTS

Computer-Aided Verification, Computer-Aided Design, Evolutionary Computation, and Artificial Life.

EDUCATION

University of Vermont, Burlington, VT
MS, Computer Science, May 2006
GPA: 4.0
Thesis: *Reduction of Redundancy in Directed Random Verification through Checkpointing*
Advisor: Craig Damon

George Washington University, Washington D.C.
Certificate, Project Management, June 2001

University of Massachusetts, Amherst, MA
BS, Computer Science, June 2000
Graduated Cum Laude

PROFESSIONAL EXPERIENCE

Staff Verification Engineer, July 2006 – Present
IBM Microelectronics, Essex Junction, VT
Verified an implementation of the PCI-Express specification using directed random verification. Founded a Design Patterns discussion group to foster better software engineering practices. Introduced statistical results analysis to the verification methodology.

Staff Physical Design Engineer, August 2001 – July 2006
IBM Microelectronics, Essex Junction, VT
Implemented numerous ARM processors in technologies ranging from 180nm to 65nm. Lead the development of IBM's first 3rd party library based digital hard IP. Created cutting-edge deep-submicron methodologies and tooling for the design of hard IP.

Software Engineer, July 2000 – August 2001
IBM Microelectronics, Essex Junction, VT
Developed Linux device drivers for a new Parallel-ATA controller. Augmented the Linux kernel to enable unique design features of the controller including out-of-order IO and advanced power management.

Research Assistant, November 1998 – June 1999
LASER, University of Massachusetts, Amherst, MA
Researched and implemented aspects of a generic agenda management system called *LittleJIL*. Developed a generic agenda viewer in Java based on introspection.

RESEARCH PUBLICATIONS

J. Craig. Functional Verification Acceleration through the Removal of Redundant Simulation. *Pending acceptance to the 44th Annual Design Automation Conference*.

N. Pratt, J. Craig, D. Jayasree, S. Jinagar. Avoiding the Pitfalls of Polymorphism. In *Proceedings of the 2006 Boston SNUG Conference*, September 2006.

J. Craig, D. Powell. Effects of Specialized Clock Routing on Clock Tree Timing, Signal Integrity, and Routing Congestion. In *Proceedings of the 2005 San Jose SNUG Conference*, March 2005.

J. Craig, S. Lovejoy. A Method for the Evolution of Transistor Placement in CMOS Cells. In *Genetic Algorithms at the University of Illinois Urbana-Champaign (IlliGAL Report No. 2001002)*, January 2001.

PATENTS

D. Chou, J. Craig, J. Sargis, D.J. Singley, S. Ventrone. *Dynamic Instruction Stream Selection in Reconfigurable Architectures*. File Pending.

J. Craig, S. Stanski, S. Vento, A. Wienick. *Acceleration of Directed Random Verification Through a Genetic Algorithm*. Filed in US May 2006.

J. Craig, S. Stanski, S. Vento. *Multi-Arm Disk Drive System Having Interleaved Read-Write Operations and Method of Controlling Same*. Filed in US Mar. 2006.

J. Craig, S. Granato, F. Kampf, B. Powers. *Testcase Harvesting in Functional Verification*. Filed in US Feb. 2006.

J. Craig, J. Norman. *Functional Coverage Acceleration Through Checkpointing and Removal of Simulation Redundancy*. Filed in US Sept. 2005, in Patent Cooperation Treaty Sept. 2006.

ADDITIONAL PRESENTATIONS

Guest Lecturer, School of Computer Science, University of Vermont, Burlington VT
CS101, Computer Organization, Fall 2006
Instructor: Alison Pechenick

AWARDS

Best First-Time Presenter – 2005 San Jose SNUG Conference
IBM Watson Scholar
UMass Amherst Dean's List

AFFILIATIONS

ΥΠΕ (Upsilon Pi Epsilon), October 2005 – Present
Open Access Coalition VSIA Committee, September 2006 – Present